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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,728	03/09/2004	Zachary Steven Smith	200308780-1	1764

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EXAMINER	
ZAMAN, FAISAL M	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,728	SMITH ET AL.	
	Examiner	Art Unit	
	Faisal Zaman	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/20/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The references listed on the Information Disclosure Statement submitted on 20 May 2005 have been considered by the examiner (see attached PTO-1449).

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 18 and 20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. In Applicant's specification, paragraph 0023, Applicant describes a computer-readable medium as being able to take the form "of electromagnetic radiation, like that generated during radio-wave and infra-red data communications, or take the form of one or more groups of signals" (lines 15-17), and "Common forms of computer-readable medium include ... a carrier wave/pulse..." (lines 17-21).

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 9-13** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claims 9-11, the phrase "at least in part" (lines 12, 5, and 5, respectively) renders the claim(s) indefinite because the claim(s) include(s) elements not actually disclosed (those encompassed by "at least in part"), thereby rendering the scope of the claim(s) unascertainable. See MPEP § 2173.05(d).

All claims not specifically addressed are rejected due to a dependency.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1-7, 9-12, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick et al. ("Gulick") (U.S. Patent No. 6,857,033) in view of Kuo (U.S. Patent Publication No. 2004/0215867).

Regarding Claims 1, 9, and 19, Gulick discloses a system (Gulick, Figure 1, item 10, Column 3, lines 32-34) comprising a virtual bus interface (Gulick, Figure 1, item 20, Column 5 line 58 – Column 6 line 1) that produces bus-type transactions (Gulick, Figure 1, item 25, Column 4, lines 31-34 and Column 5 line 58 – Column 6 line 1) from point-to-point transactions (Gulick, Figure 1, items 15A-D and 50A, Column 3 lines 32-36, Column 4 lines 29-31, and Column 5 line 58 – Column 6 line 1).

Gulick does not expressly disclose wherein the system comprises:

A detection logic configured to detect that a point-to-point transaction to be processed by the virtual bus interface is a transaction for which no bus-type transaction is to be produced; and

A tracking logic operably connected to the detection logic, the tracking logic being configured to track the point-to-point transaction as it is processed by the virtual bus interface and to selectively suppress the generation of a bus-type transaction by a translation logic in the virtual bus interface.

In the same field of endeavor (e.g. a control chip for converting data from one bus-type to another bus-type), Kuo teaches:

A detection logic (Kuo, Figure 2, item 220, page 2, paragraph 0026) configured to detect that a bus cycle transaction to be processed by a virtual bus interface (Kuo, Figure 2, item 200, page 2, paragraph 0026) is a transaction for which no bus-type transaction is to be produced (Kuo, page 1, paragraph 0010); and

A tracking logic (Kuo, Figure 2, item 220, page 2, paragraph 0026, since all the actions concerning determining whether or not to inhibit the bus cycle occurs within the bus cycle inhibiting circuit 220 [see Kuo, page 2, paragraphs 0028-0030], it would be obvious to one of ordinary skill in the art that the bus cycle inhibiting circuit 220 also acts as a tracking logic) operably connected to the detection logic, the tracking logic being configured to track the bus cycle transaction as it is processed by the virtual bus interface and to selectively suppress the generation of a bus-type transaction by a translation logic (Kuo, Figure 2, item 210, page 2, paragraph 0027) in the virtual bus interface.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Kuo's teachings of a control chip for converting data from one bus-type to another bus-type to the teachings of Gulick, for the purpose of reducing wasted cycle time and saving electrical power (see Kuo, page 1, paragraph 0007). Gulick also provides motivation to combine by stating it is an object of the invention to increase the bandwidth in a shared bus system by decreasing the electrical capacitance on the bus (see Gulick, Column 1, lines 22-33 and Column 2, lines 8-17).

Regarding Claim 2, Gulick discloses a detection logic (ie. I/O node 20) that examines a packet identifier in a header packet associated with the point-to-point transaction (Gulick, Column 6, lines 2-5 and lines 8-27).

Gulick does not expressly disclose wherein the detection logic is configured to detect that a point-to-point transaction is a transaction for which no

bus-type transaction is to be produced by examining a packet identifier in a header packet associated with the point-to-point transaction.

In the same field of endeavor, Kuo teaches a detection logic (Kuo, Figure 2, item 220, page 2, paragraph 0026) that is configured to detect that a bus cycle transaction is a transaction for which no bus-type transaction is to be produced by examining an incoming bus cycle (Kuo, page 1, paragraph 0010).

The motivation that was utilized in the combination of Claim 1, super, applies equally as well to Claim 2.

Regarding Claims 3-5 and 10-12, Kuo teaches where the tracking logic is configured to suppress the generation of a bus-type transaction by the translation logic in the virtual bus interface by updating a value in a data structure or data store associated with tracking the point-to-point transaction (ie. bus cycle transaction, see discussion of Claim 1 above) or by marking the point-to-point transaction with a suppression tag, where the value or tag is referenced by the translation logic before providing a bus-type transaction (Kuo, page 2, paragraphs 0029-0030, "register 241 is a storage device for holding a value for enabling internal bus cycle inhibition").

The motivation that was utilized in the combination of Claim 1, super, applies equally as well to Claims 3-5.

Regarding Claim 6, the examiner takes Official Notice that the use of a null-type transaction in a point-to-point transaction in the type of system

disclosed was well-known in the art at the time of Applicant's invention and the use of it would not affect the scope of the invention. Therefore, it would obvious to one of ordinary skill in the art to use any type of transaction, including a null-type transaction in the disclosed system.

Regarding Claim 7, Kuo teaches where the point-to-point transaction (ie. the bus cycle transaction, see discussion of Claim 1 above) comprises a point-to-point internal transaction (Kuo, page 1, paragraph 0010, "an internal bus cycle type").

Claim Rejections - 35 USC § 103

7. **Claims 8 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick-Kuo as applied to Claim 1 above, in further view of Martino (U.S. Patent No. 5,805,676).

Regarding Claim 8, Gulick-Kuo teaches where a detection logic is configured to receive an input (Kuo, page 1, paragraph 0010, "bus cycle") that identifies a point-to-point transaction type to be suppressed (Kuo, page 1, paragraph 0010, "an internal bus cycle type").

Gulick-Kuo does not expressly disclose wherein the detection logic is configured to receive an input from a user, where the input identifies a point-to-point transaction type to be suppressed.

In the same field of endeavor (e.g. a data transaction processing system), Martino teaches a detection logic configured to receive an input from a user, where the input identifies a transaction type (Martino, Column 26, lines 19-42).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Martino's teachings of a data transaction processing system to the teachings of Gulick-Kuo, for the purpose of performing operations with a minimal amount of processing (see Martino, Column 2, lines 10-15). Gulick-Kuo also provide motivation to combine by stating it is an object of the invention to reduce wasted cycle time and save electrical power (see Kuo, page 1, paragraph 0007).

Regarding Claim 13, all the same elements of Claims 6-8 are listed, but grouped into a single claim rather than three separate claims. Therefore, the supporting rationale of the rejection to claims 6-8 apply equally as well to Claim 13.

Claims 14-17 are directed to a method of the system of Claims 1-8, **Claim 18** is directed to a computer-readable medium operable to perform the method of the system of Claims 1-8, and **Claim 20** is directed to a set of application programming interfaces embodied on a computer-readable medium for execution on the system of Claims 1-8. Gulick, Kuo, and Martino teach, either alone or in combination as stated above, the system as set forth in Claims 1-8. Therefore, Gulick, Kuo, and Martino also teach, either alone or in combination as stated

above, a method as set forth in Claims 14-17, a computer-readable medium as set forth in Claim 18, and a set of application programming interfaces embodied on a computer-readable medium as set forth in Claim 20.

Prior Art of Record

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Zeller et al. (U.S. Patent No. 5,761,725) discloses a cache-based computer system employing a peripheral bus interface unit with cache write-back suppression and processor-peripheral communication suppression for data coherency. Vogt et al. (U.S. Patent No. 5,897,656) discloses a system and method for maintaining memory coherency in a computer system having multiple system buses. Uehara et al. (U.S. Patent Publication No. 2002/0040414) discloses a multiprocessor system and transaction control method for the same. Owen et al. (U.S. Patent Publication No. 2002/0103945) discloses a system and method of initializing a computer processing system having a plurality of point-to-point links interconnecting a plurality of devices. Pekkala et al. (U.S. Patent Publication No. 2002/0172195) discloses an apparatus and method for disparate fabric data and transaction buffering within an Infiniband device. Wang et al. (U.S. Patent No. 6,516,442) discloses a channel interface and protocol for cache coherency in a scalable symmetric multiprocessor system. Wang et al. (U.S. Patent Publication No. 2003/0110338) discloses a method and apparatus for emulating computer buses using point-to-

point techniques. Vogt et al. (U.S. Patent No. 6,622,214) discloses a system and method for maintaining memory coherency in a computer system having multiple system buses. Ludwig et al. (U.S. Patent No. 6,697,352) discloses a communication device and method. Swarbrick et al. (U.S. Patent Publication No. 2004/0114609) discloses an interconnection system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal Zaman whose telephone number is 571-272-6495. The examiner can normally be reached on Monday thru Friday, 9 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

FMZ

Khanh Dang
Primary Examiner